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Aboushady, Ahmed; Finney, Stephen; Williams, Barry; Ahmed, Khaled

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Steady State Analysis of the Phase-Controlled LCC-type Series-Parallel Resonant Converter Operating Above Resonance

A.A.Aboushady, S.J.Finney, and B.W.Williams
Department of Electrical and Electronics Engineering
University of Strathclyde
Glasgow, United Kingdom
ahmed.aboushady@eee.strath.ac.uk

K.H.Ahmed
School of Engineering
University of Aberdeen
Aberdeen, United Kingdom
khaled@abdn.ac.uk

Abstract—This paper presents a new analysis providing further insight into the steady state characteristics of the phase-controlled LCC-type series-parallel resonant converter operating above resonance. An analytical expression is obtained for the converter voltage transfer function in terms of phase angle. The effect of varying the phase angle on ZVS and ZCS of the inverter switches is studied and, accordingly, converter modes of operation are classified and illustrated. Mode boundaries are analytically derived and graphically represented to ease the determination of converter operating mode at any loading, frequency and phase angle combination. Finally, maximum power transfer criterion is obtained and plotted for the converter. The analysis presented is helpful with converter design and determination of the suitable operating conditions.

I. NOMENCLATURE

v_s	DC link supply voltage (V)
v_{AB}	Inverter output voltage (V)
n	Transformer turns ratio
v_{AB}'	Inverter output voltage referred to secondary = nv_{AB} (V)
v_{AB1}	Fundamental inverter output voltage (V)
L_s	Resonant tank inductance (μ H)
L_l	Transformer leakage inductance referred to secondary (μ H)
L_T	Total equivalent inductance $L_T = L_l + L_s$ (μ H)
C_s	Resonant tank series capacitance (μ F)
C_p	Resonant tank parallel capacitance (μ F)
L_o	Output filter inductance (mH)
C_o	Output filter capacitance (μ F)
ω	Inverter switching frequency (rad/s)
ω_0	Series circuit resonance frequency = $1 / 2\pi\sqrt{L_T C_s}$ (rad/s)
ω_{pu}	Normalized frequency = ω / ω_0
i_L	Resonant tank inductor current (A)
v_{Cs}	Resonant tank series capacitor voltage (V)

v_{Cp}	Resonant tank parallel capacitor voltage (V)
i_{Br}	Bridge rectifier input current (A)
v_o	Output voltage (V)
i_o	Output current (A)
R_L	Load resistance (Ω)
R_{ac}	AC equivalent resistance of bridge rectifier = $(\pi^2 / 8)R_L$ (Ω)
δ	Phase angle (rad) $0 \leq \delta \leq \pi$
Z_c	Resonant tank characteristic impedance = $\sqrt{L_T / C_s}$ (Ω)
Q	Quality factor = $\omega_0 L_T / R_L = Z_c / R_L$

II. INTRODUCTION

Steady state characteristics of the variable and fixed frequency controlled series-parallel resonant converter (SPRC) have been analyzed extensively in literature. Variable frequency operated LCC-type SPRC with half-bridge inverters [1-3] or class D resonant inverters [4] are thoroughly analyzed at steady-state. However, variable frequency operation presents practical disadvantages, like a wide noise spectrum which makes it difficult to control EMI, more complex filtering and poor utilization of magnetic components. For this reason, fixed frequency operation like phase-shift control of SPRC overcomes problems of variable frequency control and offers good control on output voltage.

Steady state analysis of the fixed frequency PWM LCC-type SPRC was studied by Bhat [5]. The latter provides simple analysis and design procedure for the converter using the complex ac circuit theory. Converter voltage transfer function was presented analytically without further steady state characteristics. Kazimierczuk [6,7] has proposed fixed frequency phase-controlled SPRCs using two paralleled class D or class E resonant inverters together with an output rectifier. Detailed steady state analytical and graphical studies of the proposed converters were carried out. However, a high

number of resonant tank components are in use compared to the simple LCC-type SPRC. Jain [8,9] has presented a phase-shift modulated double tuned LLCC-type SPRC to reduce conduction and switching losses of the conventional LCC-type SPRC and hence obtain better efficiency for wide input voltage and output load variations. Again, more resonant components are in use.

This paper presents a new analysis providing further insight into the basic phase-controlled LCC-type SPRC considering the effect of varying the phase angle, output load and switching frequency above resonance on converter operation. Detailed converter modes of operation are analyzed and the boundaries between them are analytically and graphically represented. Conditions for maximum power transfer to load are also derived, discussed and illustrated graphically.

III. CIRCUIT DESCRIPTION

Fig.1 depicts the phase-controlled SPRC circuit diagram. For the sake of simplicity, it is assumed that the resonant inductor current is sinusoidal due to the low pass filter effect of the resonant tank operating above resonance. This means that power from the inverter is transferred to load solely at fundamental frequency. Output filter inductor L_o is large enough to keep load current constant. The effect of all parasitics, transformer magnetizing inductance, and inverter snubbers are neglected. Parallel resonant capacitor C_p is equal to the series resonant capacitor C_s . Using this assumption, the SPRC comprises the advantages of the series- and parallel-resonant converters and eliminates their operational problems.

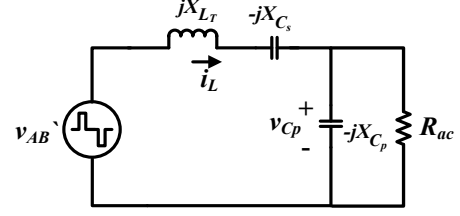
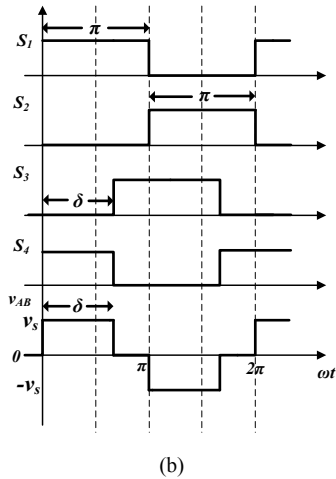
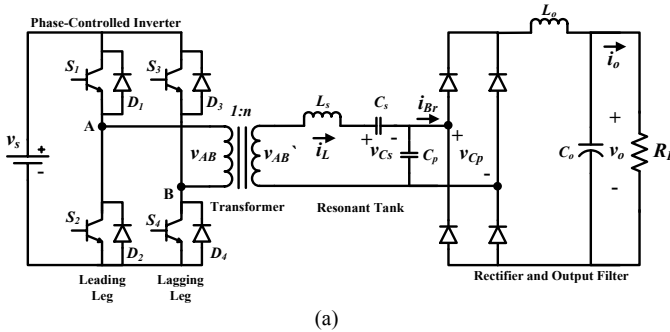


Fig.1. LCC-type series-parallel resonant converter (a) circuit diagram (b) inverter gating pattern, and (c) ac equivalent circuit.

IV. VOLTAGE GAIN TRANSFER FUNCTION

Using the ac equivalent circuit in Fig.1(c), the voltage transfer function of the SPRC can be derived,

$$\frac{|v_{Cp}|}{|v_{AB}|} = \frac{1}{\left(1 + \frac{X_{Cs}}{X_{Cp}} - \frac{X_{LT}}{X_{Cp}}\right) + j\left(\frac{X_{LT}}{R_{ac}} - \frac{X_{Cs}}{R_{ac}}\right)} \quad (1)$$

where, v_{AB} and v_{Cp} are the fundamental inverter output voltage referred to transformer secondary and parallel capacitor voltages respectively. Using Fourier transform, equation (1) can be represented as

$$\left(\frac{\pi}{2} v_o\right) = \frac{1}{\left(1 + \frac{X_{Cs}}{X_{Cp}} - \frac{X_{LT}}{X_{Cp}}\right) + j\left(\frac{X_{LT}}{R_{ac}} - \frac{X_{Cs}}{R_{ac}}\right)} \quad (2)$$

Applying the definitions of R_{ac} , Q and ω_0 in nomenclature, and for $C_p = C_s$ equation (2) can be expressed as

$$M = \frac{v_o}{v_s} = \frac{n \sin \frac{\delta}{2}}{\left[\frac{\pi^2}{8} (2 - \omega_{pu}^2) + jQ \left(\omega_{pu} - \frac{1}{\omega_{pu}}\right)\right]} \quad (3)$$

where, M is the converter voltage gain plotted in Fig.2 for above resonance operation ($\omega_{pu} > 1$) and unity transformer turns ratio ($n=1$).

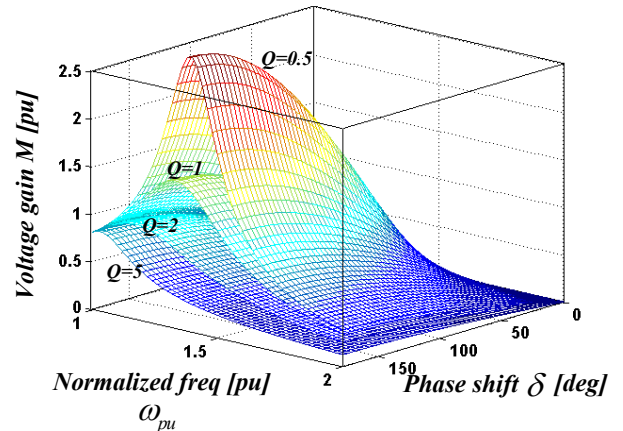


Fig.2. Converter voltage gain M

The converter can operate in step up or down modes depending on the loading factor Q and inverter switching frequency. Generally higher gains are obtained with light loads (low Q) with the resonant frequency boundary between inductive and capacitive resonant circuit shifting from ω_0 to

$$\omega_{02} = 1 / \sqrt{\frac{L_T C_p C_s}{C_p + C_s}} \text{ at no load. This reduces to } \omega_{02} = \sqrt{2} \omega_0 \text{ for } C_p = C_s$$

which is shown in Fig.2 by the peak gain at $Q=0.5$ and $\omega_{pu}=1.414$. The gain is reduced significantly for increased frequencies, reduced phase shift and for heavy loads with high Q factors.

V. MODES OF OPERATION

Four modes of converter operation exist for the phase-controlled LCC-type SPRC operating above resonance. These modes are summarized in Table I and depended on whether the resonant circuit is inductive or capacitive (according to loading factor Q and inverter operating frequency ω_{pu} above resonance as well as the magnitude of phase-shift angle δ). A few important parameters to define are:

- Input impedance of resonant circuit as from Fig. 1(c)

$$Z = \frac{R_{ac} X_{C_p}^2 + j \left[R_{ac}^2 (X_{L_T} - X_{C_s} - X_{C_p}) + X_{C_p}^2 (X_{L_T} - X_{C_s}) \right]}{R_{ac}^2 + X_{C_p}^2} \quad (4)$$

- Input impedance angle for $C_p = C_s$

$$\phi_z = \tan^{-1} \left[\frac{\omega_{pu}^4 + \left(\frac{64Q^2}{\pi^4} - 2 \right) \omega_{pu}^2 - \frac{64Q^2}{\pi^4}}{\frac{8Q}{\pi^2} \omega_{pu}} \right] \quad (5)$$

- Resonant circuit frequency for $C_p = C_s$ (obtained by $\text{Imag}(Z)=0$)

$$\omega_{res(pu)} = \frac{\omega_{res}}{\omega_0} = \sqrt{\left(1 - \frac{32Q^2}{\pi^4}\right)} + \sqrt{\left(1 - \frac{32Q^2}{\pi^4}\right)^2 + \frac{64Q^2}{\pi^4}} \quad (6)$$

For mode comparisons, Fig. 3 shows the equivalent steady state ac circuits for a positive half cycle of the inverter output voltage v_{AB} . Negative half cycle equivalent circuits are identical but with $-v_s$ and the complementary inverter switches conducting. Mode operations are explained as follows:

A. Mode 1:

During sub-period A , resonant inductor current is negative; hence, resonant tank energy is fed back to the dc supply through diodes D1, D4. At the end of sub-period A , the resonant inductor current falls to zero and the powering stage starts with sub-periods B and C where energy is transferred from the source to the tank through switches S1, S4. During sub-period B , parallel capacitor C_p discharges until $v_{Cp}=0$. In sub-period C , $i_L > i_o$ and C_p charges up; hence the rapid rise in v_{Cp} . Correspondingly the inductor voltage decreases, allowing the inductor current to start decay.

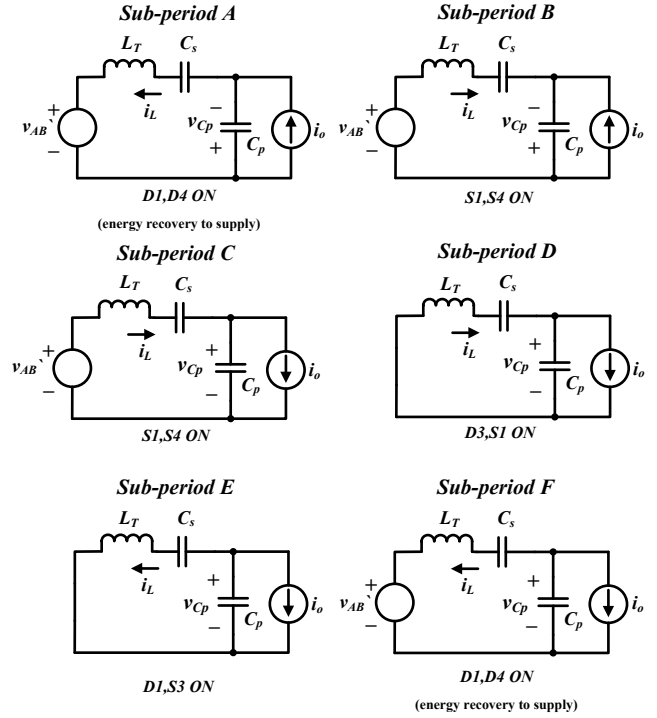


Fig. 3. Equivalent ac circuits for the positive half-cycle sub-periods

During sub-period D , the inverter upper half conducts (D3, S1). Energy in the resonant tank is dissipated in the zero voltage loop and no energy is returned to the dc supply.

Converter switch voltage/current waveforms, verify zero-voltage turn on for all four switches in this mode of operation. The load current is carried by the switch antiparallel diode prior to switch operation hence the voltage across it is zero before conduction of the forward current. All four switches turn off whilst conducting current, but with inverter lagging leg switches turning off higher current. Switching stresses are therefore higher on the lagging leg compared to the leading leg.

This mode is characterized by the resonant inductor current i_L lagging the fundamental inverter output voltage v_{AB1} since $\omega_{pu} > \omega_{res(pu)}$ which means that the resonant tank is inductive and operation is on the negative slope of the frequency response plot. However, this mode is differentiated from mode 2 by the fact that i_L is also lagging the positive-going edge of the inverter output voltage waveform (v_{AB}), that is $\phi_z < \frac{\pi - \delta}{2}$.

B. Mode 2:

As explained in mode 1 operation, mode 2 is characterized by a leading i_L waveform relative to the positive-going edge of v_{AB} while still lagging the fundamental v_{AB1} waveform. Operation is on the negative frequency response slope but zero voltage turn on is lost for the inverter leading leg switches only. Leading leg switches such as S1 turn on with positive current and ZVS is lost. The negative turn off current in S1 (through D1, S3, sub-period E) flows through S2, S3 at the start of the negative half cycle powering stage. The reverse recovery time of D1 must, therefore, be

short to prevent overlapping conduction with S2 in the same leg. This necessitates the use of fast recovery free wheel diodes for the leading leg switches in mode 2. No energy is recovered to the supply during this mode. Inverter lagging leg switches operate in a similar manner to mode 1 with zero voltage turn on.

C. Mode 3:

When operation is below resonance ($\omega_{pu} < \omega_{res(pu)}$), the resonant circuit becomes capacitive and i_L leads the fundamental inverter output voltage v_{AB1} . Similar to mode 1, energy is recovered to the supply through diodes D1, D4 (sub-period F) due to i_L leading the negative-going edge of inverter output voltage waveform v_{AB} . Operation is on the positive slope of the frequency response plot and all the inverter switches turn on positive current while turn off occurs at zero voltage. This necessitates the use of fast recovery diodes for all inverter switches (not only leading leg switches like in mode 2).

D. Mode 4:

Operation is below resonance ($\omega_{pu} < \omega_{res(pu)}$) but with i_L lagging the negative-going edge of v_{AB} . This means that no energy is recovered to the supply in this mode. Instead energy is dissipated in the zero-voltage loops of sub-periods D and E . Operation is on the positive slope of the frequency response plot but now with the inverter lagging leg switches switching on at zero-voltage. Only the leading leg switches turn on positive current, meaning that, similar to mode 2, fast recovery diodes are mandatory only for the leading leg switches.

Typically mode 1 is preferable due to the ZVS of both inverter legs. Switch turn on losses are eliminated and turn off losses can be mitigated by the use of lossless capacitive snubbers. Contrarily, operating below resonance (as in mode 3) results in transistor turn on switching losses and diode switching losses (fast recovery diodes are needed). Transistor turn off does occur in a lossless manner when operating below resonance. However, because turn off losses can be reduced using lossless snubbers when operating above resonance, this is not a major argument for operating below resonance. Fig. 4 illustrates the mode boundary conditions defined by the last column of Table I.

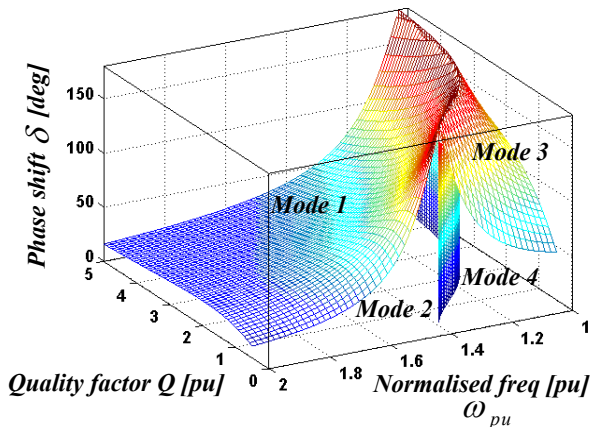


Fig. 4. Mode boundaries

Mode 1 operation is guaranteed for a wide load range for $\omega_{pu} > \sqrt{2}$ provided δ is not too low; otherwise mode 2 occurs. However, for $1 < \omega_{pu} < \sqrt{2}$ mode 1 occurs only for heavier loads. At lighter loads, mode 4 is preferred to mode 3 due to the lagging leg operating with ZVS. Therefore it can be concluded that operating at $\omega_{pu} > \sqrt{2}$ guarantees the preferred operation region (mode 1 for a wide load range or mode 2 in the worst case at excessively low δ). On the other hand, excessive increase in switching frequency leads to reduced converter voltage gain as illustrated in Fig. 2. Fig. 5 shows experimental results for a 40 kHz phase-controlled SPRC to verify the mode boundary relations in Fig. 4 at different operating conditions.

VI. MAXIMUM POWER TRANSFER

Maximum power transfer occurs when the load impedance matches the Thevenin equivalent impedance of the resonant tank. Hence, considering Fig. 1(c), maximum power transfer can be obtained by,

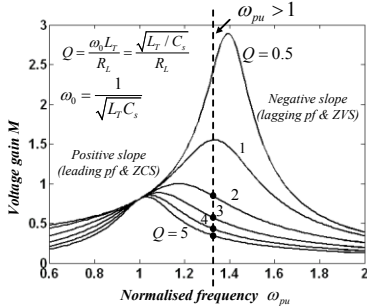
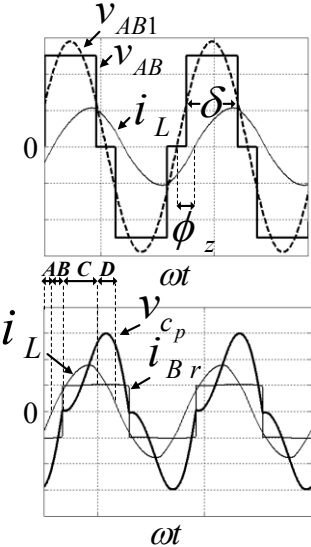
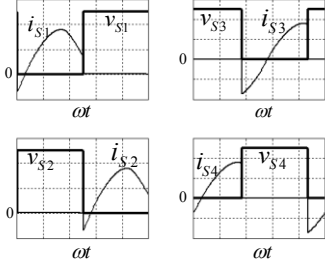
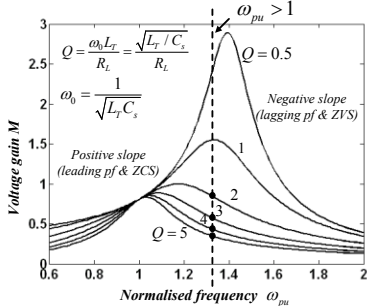
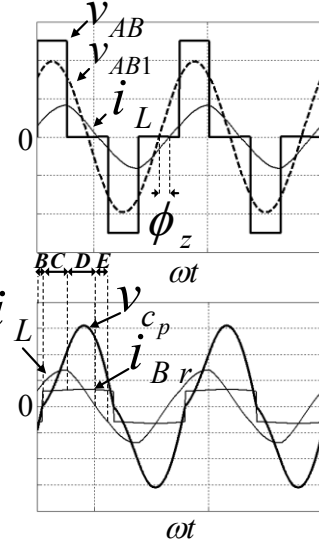
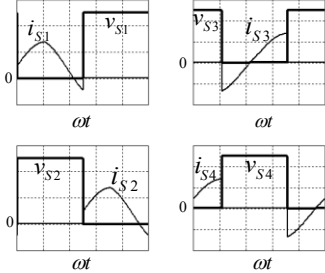
$$R_{ac} = \left| \frac{-jX_{C_p} * j(X_{L_T} - X_{C_s})}{j(X_{L_T} - X_{C_s} - X_{C_p})} \right| \quad (7)$$

Equation (7) can be re-formulated using the definitions of R_{ac} , Q and ω_{pu}

$$Q = \frac{\omega_{pu}^2 - 2}{\frac{8}{\pi^2} \left(\omega_{pu} - \frac{1}{\omega_{pu}} \right)} \quad (8)$$

Per unit converter output power is plotted in Fig. 6. From (8), for every switching frequency there exists a value of Q where maximum power transfer occurs. At heavy loads (high Q), maximum power transfer occurs near $\omega_{pu}=1$ where the circuit is purely resistive since the load effectively shorts the parallel capacitor C_p , hence the circuit acts as a series resonant converter. As load gets lighter, resonance is asymptotic to $\omega_{pu}=1.414$ where maximum power transfer occurs. For $\omega_{pu}>1.414$, low Q is preferred for maximum power transfer since the circuit is analogous to a parallel resonant converter. Maximum power transfer in (8) is seen to be independent of the phase angle δ . This is inevitable as power transferred to the load is directly proportional to the converter effective duty ratio (higher phase angle).

TABLE I. MODES OF OPERATION OF THE PHASE-CONTROLLED SPRC OPERATING ABOVE RESONANCE

	Mode	Leading leg (S_1S_2)	Lagging leg (S_3S_4)	Location on frequency response plot	Voltage/Current waveforms		Energy recovery to supply	Conditions for mode operation
					Resonant tank	Converter switches		
Lagging inductor current	1	ZVS	ZVS				Yes	$\omega_{pu} > \omega_{res(pu)}$ and $\phi_z > \frac{\pi - \delta}{2}$
	2	ZCS	ZVS				No	$\omega_{pu} > \omega_{res(pu)}$ and $\phi_z < \frac{\pi - \delta}{2}$

	Mode	Leading leg (S_1S_2)	Lagging leg (S_3S_4)	Location on frequency response plot	Voltage/Current waveforms		Energy recovery to supply	Conditions for mode operation
					Resonant tank	Converter switches		
Leading inductor current	3	ZCS	ZCS				Yes	$\omega_{pu} < \omega_{res}(pu)$ and $-\phi_z > \frac{\pi - \delta}{2}$
	4	ZCS	ZVS				No	$\omega_{pu} < \omega_{res}(pu)$ and $-\phi_z < \frac{\pi - \delta}{2}$

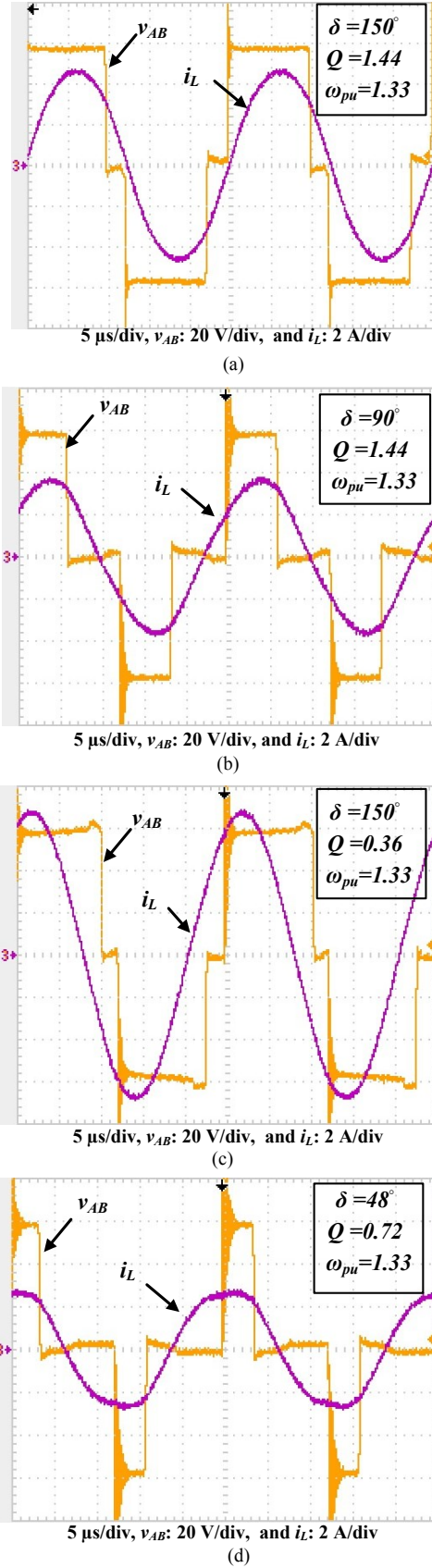


Fig. 5. Experimental results with different operating modes (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

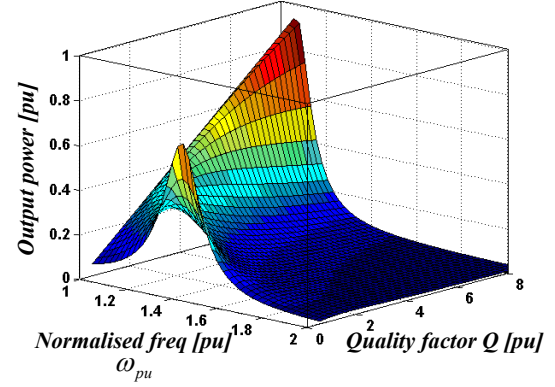


Fig. 6. Maximum power transfer

VII. CONCLUSION

This paper has presented some further insight into the operation of the phase-controlled LCC-type SPRC which aids with converter design and choice of operating conditions. For a SPRC with $C_p = C_s$, it is optimum to operate with inverter switching frequency in the range of $1 < \omega_{pu} < 1.414$. In this frequency range, a wide voltage gain range is feasible in addition to the higher possibility of operating in the preferred mode 1 with ZVS in both inverter legs for a wide load range. This not only means that switching losses are mitigated significantly but also means that fast recovery diodes are only needed for the leading inverter leg switches due to the possible ZCS operation in mode 2. The operating Q that satisfies maximum power transfer depends on choice of ω_{pu} inside the selected range. At frequencies close to $\omega_{pu} = 1$, maximum power is transferred at high Q . However, this is not really preferable since the converter voltage gain becomes very low. Unless this is a design requirement, it is preferable to operate closer to the mid-range frequency to avoid no-load resonance operation at $\omega_{pu} = 1.414$. The different modes of operation have been practically verified and confirmed.

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